

Software development for nanosatellite microcontrollers

Microcomputer



Main problems

- What tasks has our computer to execute?
- What kind of processor is the most suitable for us?
- Do we need an operating system?
- What language will we use for programming?

Approaches:

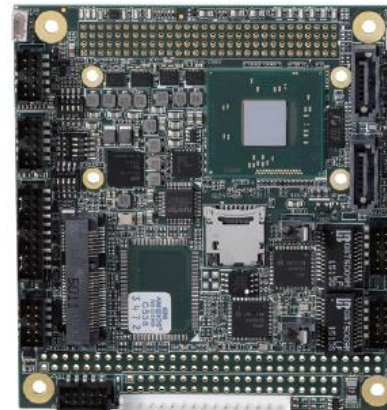
- User's specific solution
- Embedded computer
- Mezzanine boards

Embedded computer

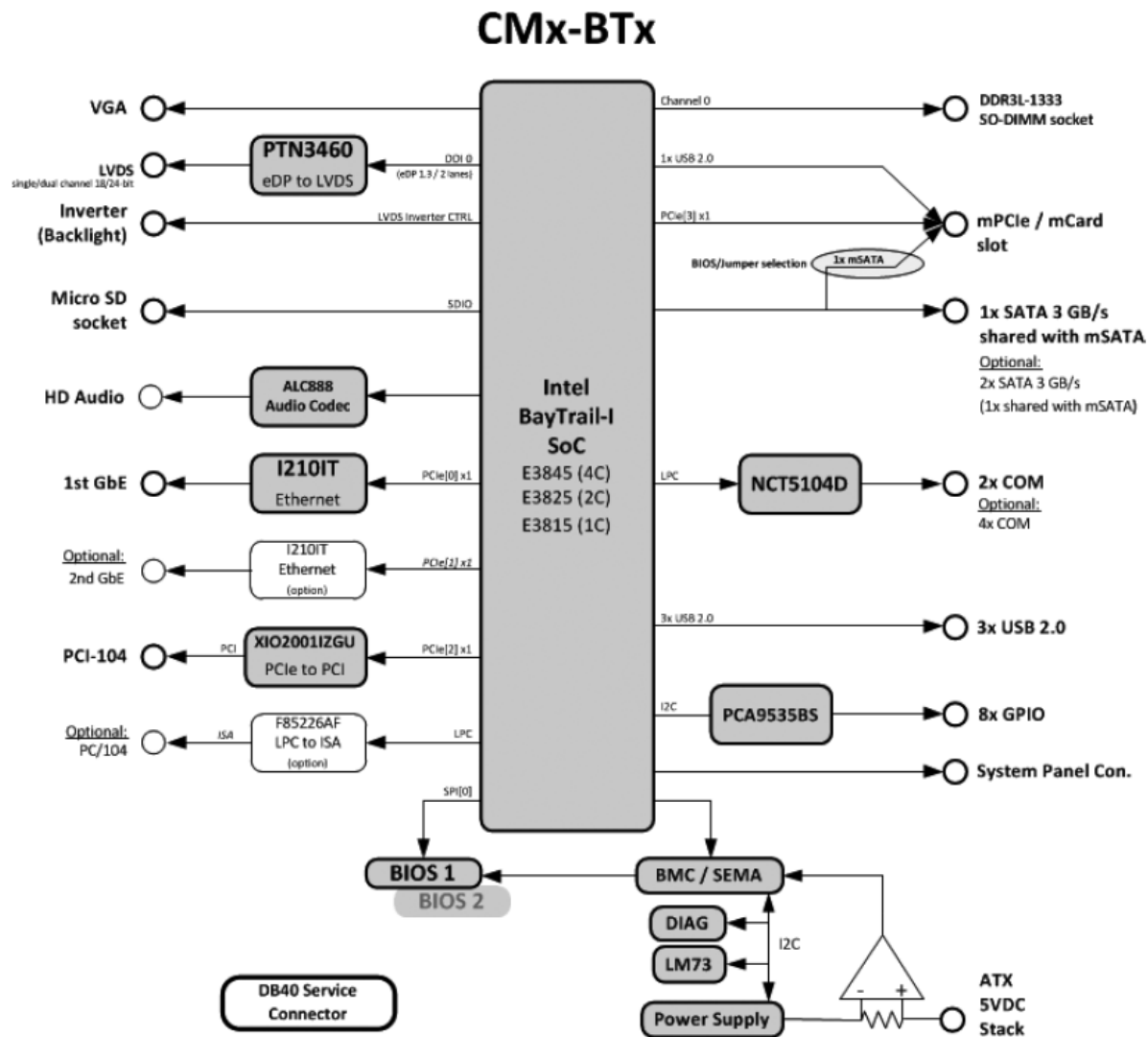
Extreme Rugged™ PCI-104 Single Board Computer with Intel Atom® Processor SoC

Features

- Quad-core Intel Atom® Processor SoC
- Up to 4GB DDR3L at 1333MHz
- Supports VGA and LVDS
- 2x GbE
- 1x SATA 3Gb/s (optional 2x SATA), 3x USB 2.0, 8x GPIO
- Extreme Rugged™ operating temperature: -40°C to +85°C
- Supports Smart Embedded Management Agent (SEMA) functions



Composition



Specifications

Specifications

- **I/O Interfaces**

- USB**

- 3x USB 2.0 (1x on mSATA)

- SATA**

- 1x SATA 3Gb/s shared with mSATA (optional 2nd SATA 3Gb/s port w/o mSATA support)

- GPIO**

- 8x

- Serial**

- 2x RS-232/422 (with full handshake) + 2x RS-232/422 (TX,RX,CTS,RTS only)

- **Power**

- Standard Input**

- ATX = 5V±5% / 5Vsb ±5% or AT = 5V±5%

- Management**

- ACPI 5.0 compliant

- Power States**

- C1-C6, S0, S3, S4, S5 (Wake on USB S3/S4, Wake on LAN S3/S4/S5)

- ECO mode**

- supports deep S5 for power saving

- **Operation System**

- Standard Support**

- Windows® 7/8 32/64-bit, Linux 32/64-bit

- Extended Support (BSP)**

- WES7/8, WEC7, Linux, QNX, VxWorks

- **Mechanical and Environmental**

- Form Factor**

- PC/104 Version 2.6

- Dimension**

- 90 mm x 96 mm

- Operating Temperature**

- Standard: 0°C to +60°C

- Extended Temperature: -40°C to 85°C (SKU dependent, by screening)

- Humidity**

- 5-90% RH operating, non-condensing

- 5-95% RH storage (and operating with conformal coating)

- Shock and Vibration**

- IEC 60068-2-64 and IEC-60068-2-27

- MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

- HALT**

- Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

- **Intelligent Middleware**

- SEMA®**



- Local management, control of embedded computer systems

- Extended EAPI for monitoring, controlling and analytics applications

- Multiple OS support and across platforms (x86, ARM)

Mezzanine boards



Key Features

- Rabbit® 3000 microprocessor @ 44.2 MHz
- 32 MB NAND Flash
- Supports up to 128 MB of hot-swappable memory
- 512K Flash/512K SRAM
- 10/100Base-T, RJ-45 port
- 52 parallel digital I/O
- 6 serial ports
- 3.3 V (with 5 V-tolerant I/O)
- Small footprint

Power	3.15–3.45 V DC 250 mA @ 44.2 MHz, 3.3 V
Operating Temperature	0° C to +70° C
Humidity	5% to 95%, non-condensing
Connectors	Two 2 × 17, 2 mm pitch One 2 × 5 for programming with 1.27 mm pitch One xD-Picture Card slot (RCM3365/RCM3375)

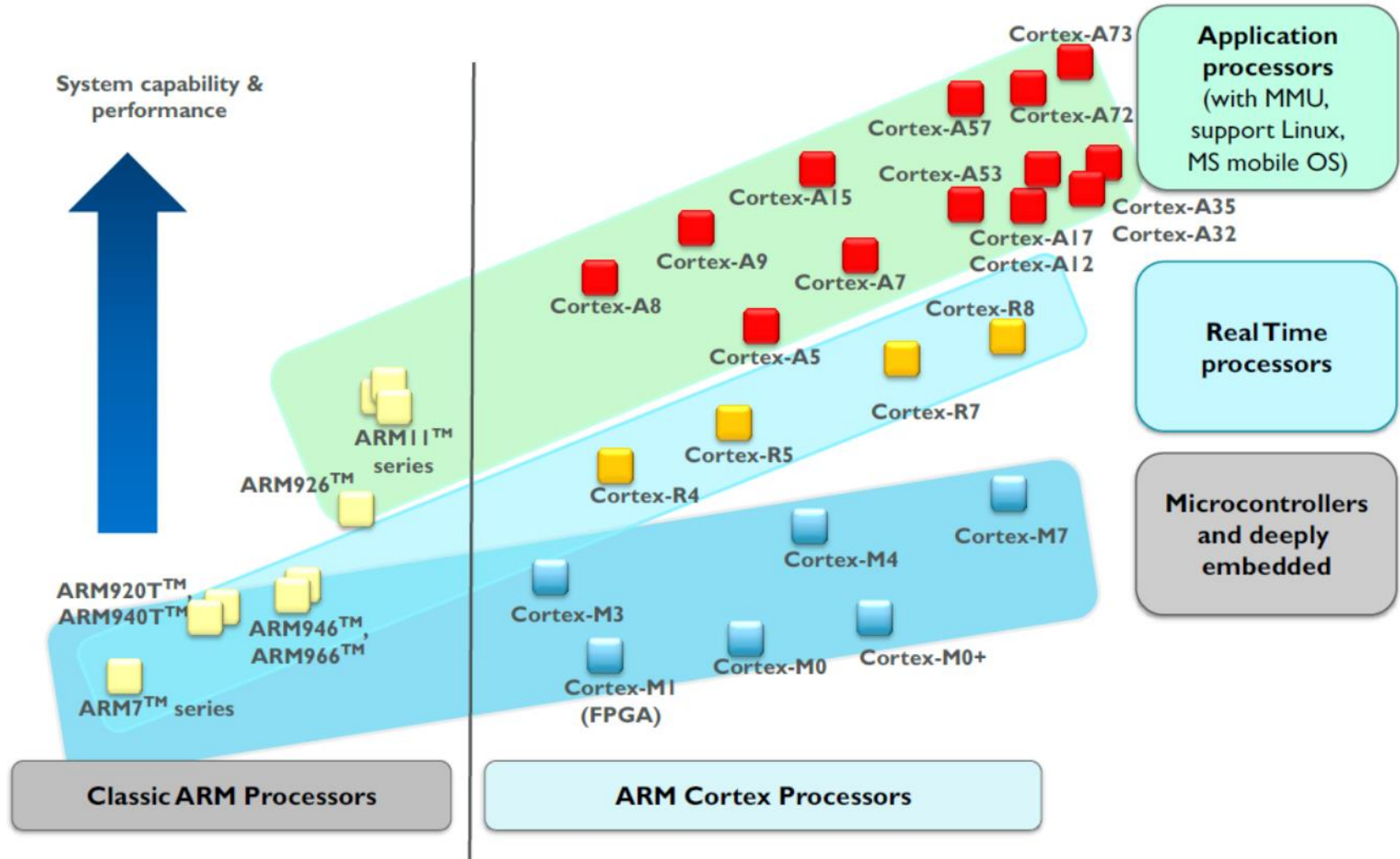
CPUs and MCUs

ARM (Advanced RISC Machines)

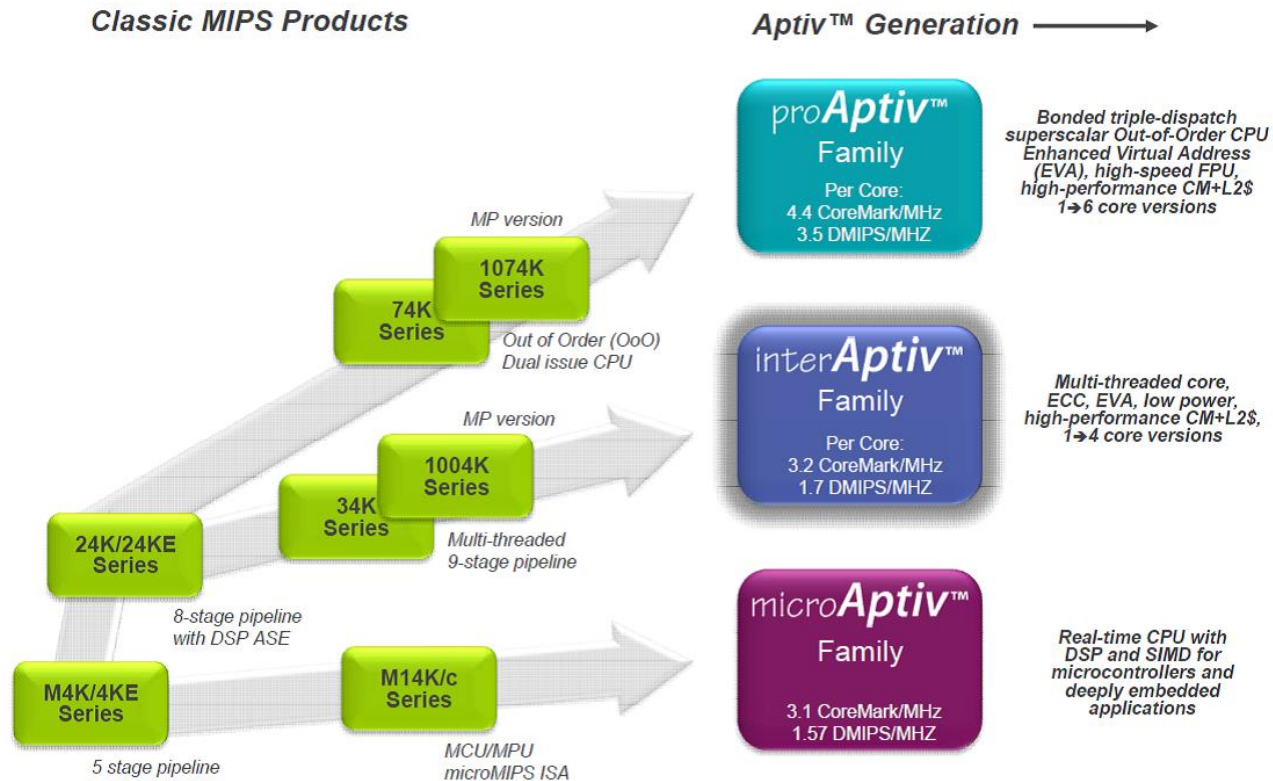
- Founded in 1990 as a joint venture of Apple Computer and Acorn Computer
- In 1991 displaced ARM6™ (Armv3)
- In 2006 - ARMv7-M (CORTEX-M3)



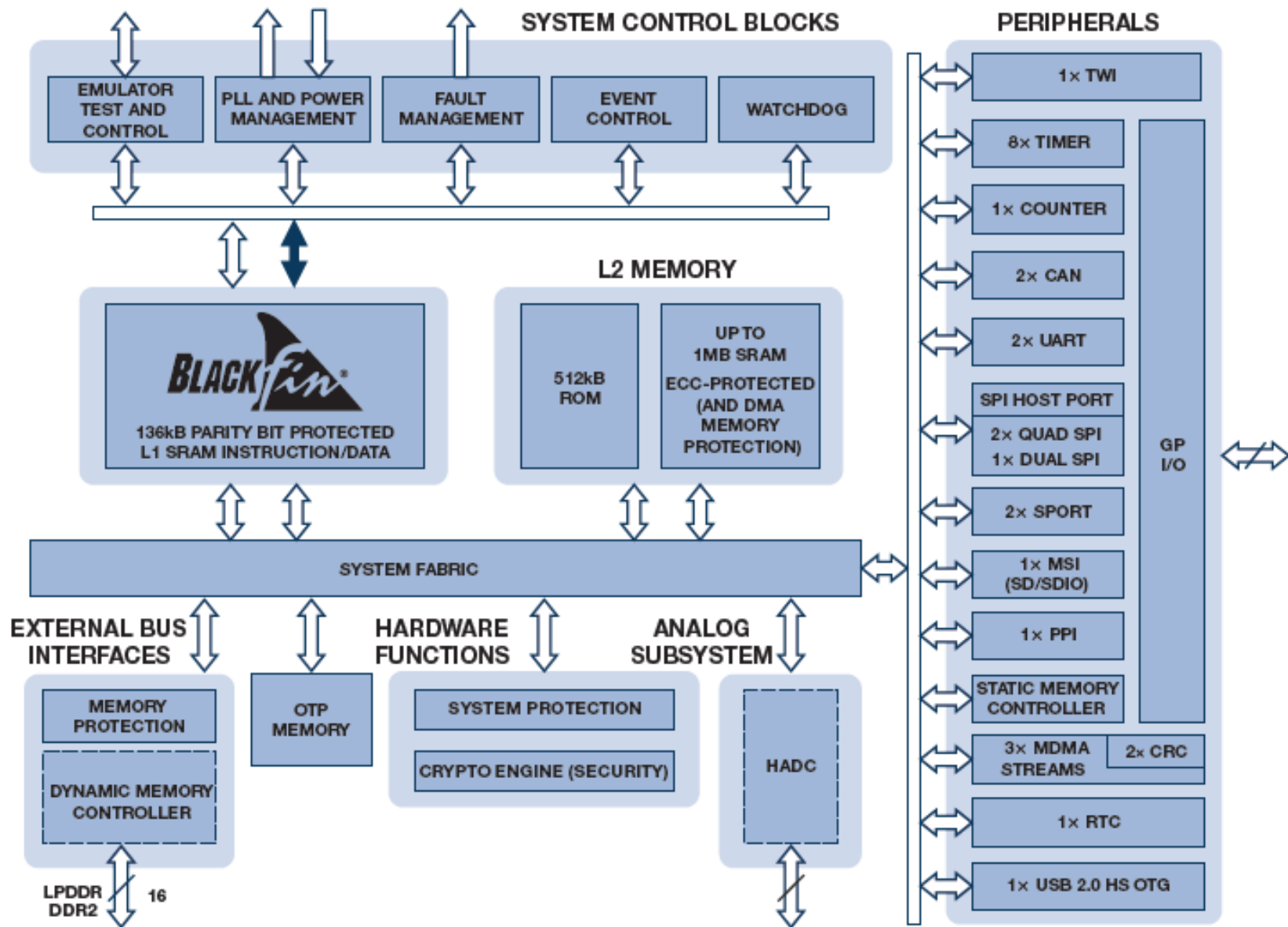
ARM ARCHITECTURES



MIPS Cores (Microchip)

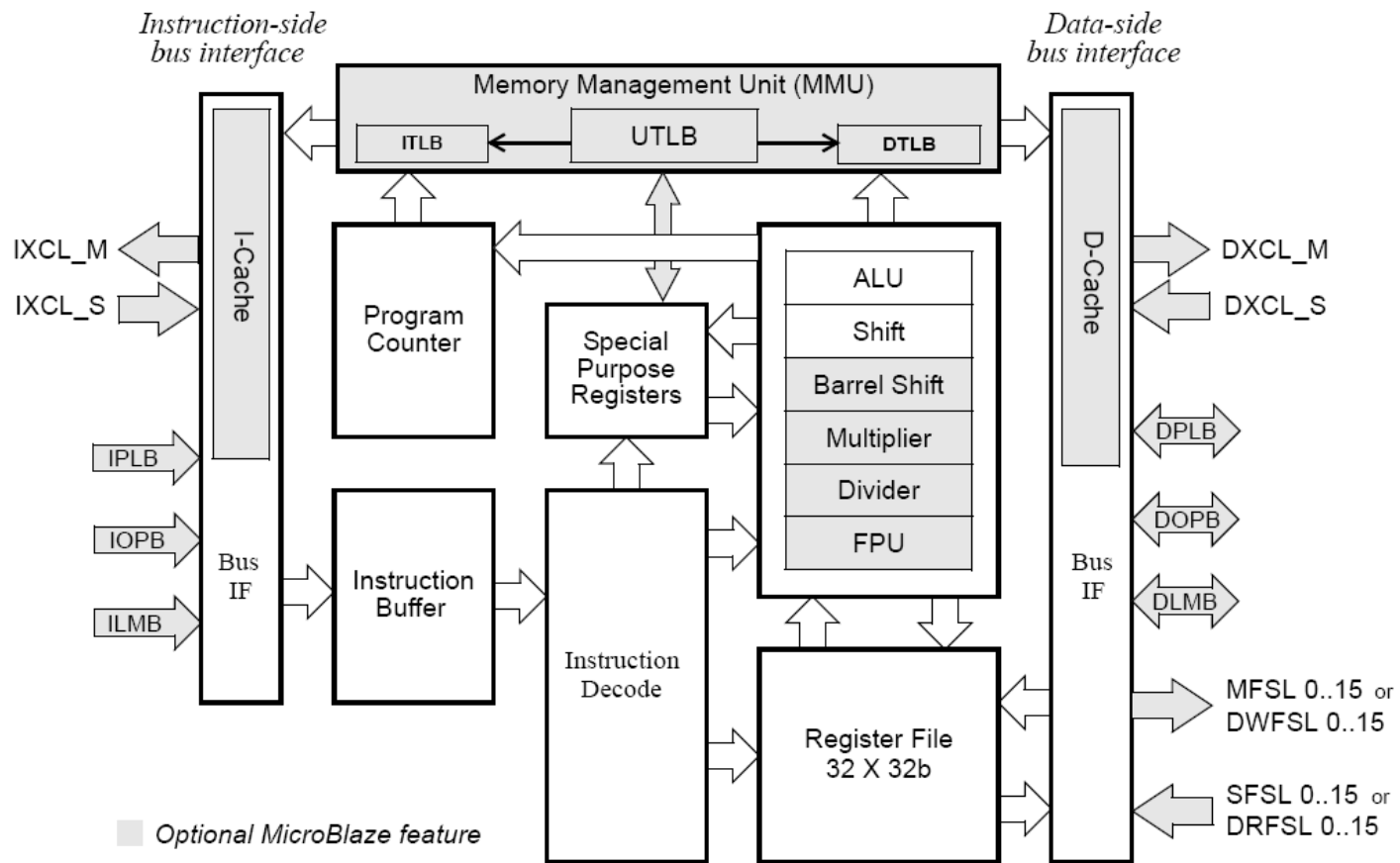


Maybe DSP ?



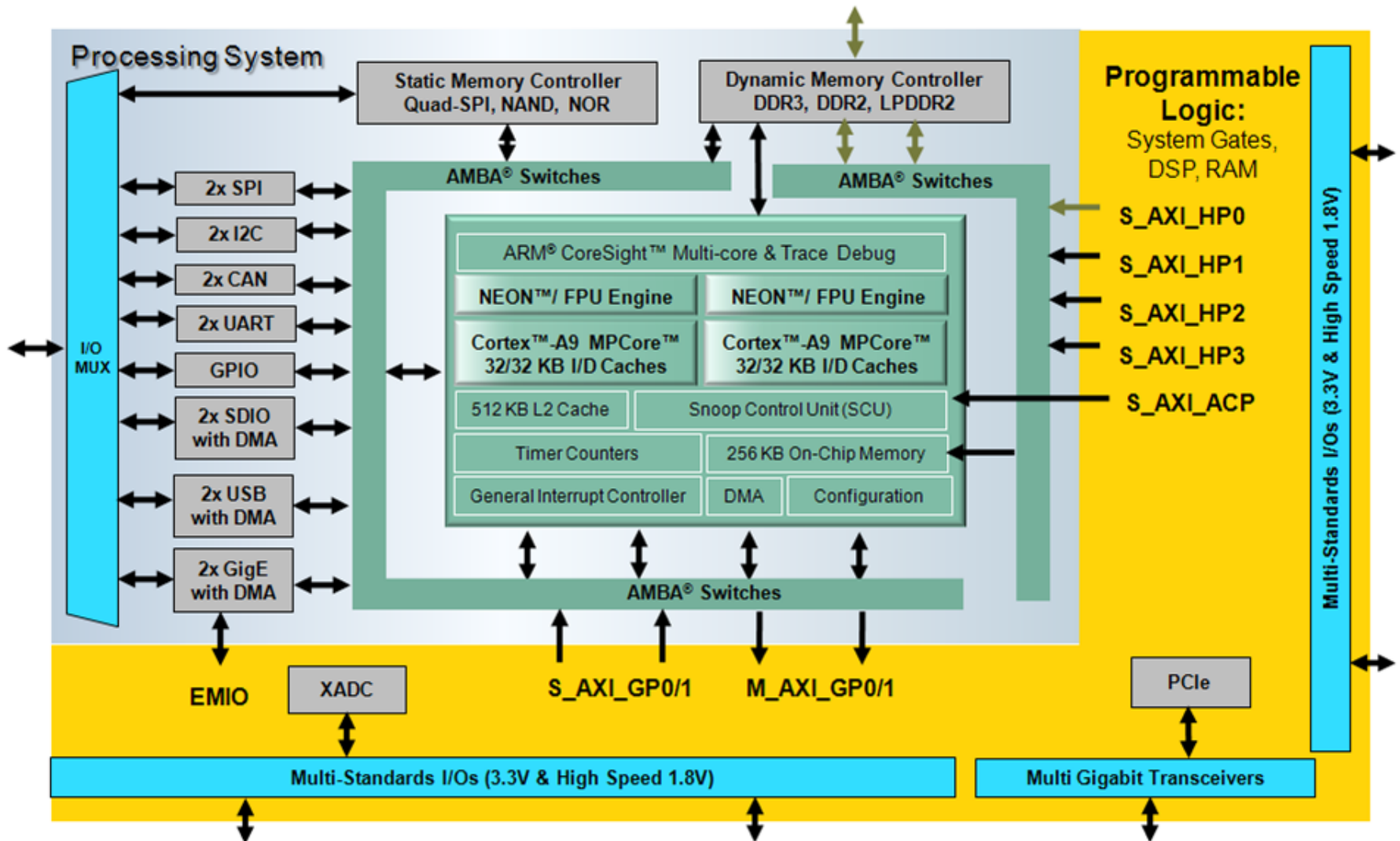
Or FPGA?

MicroBlaze Architecture

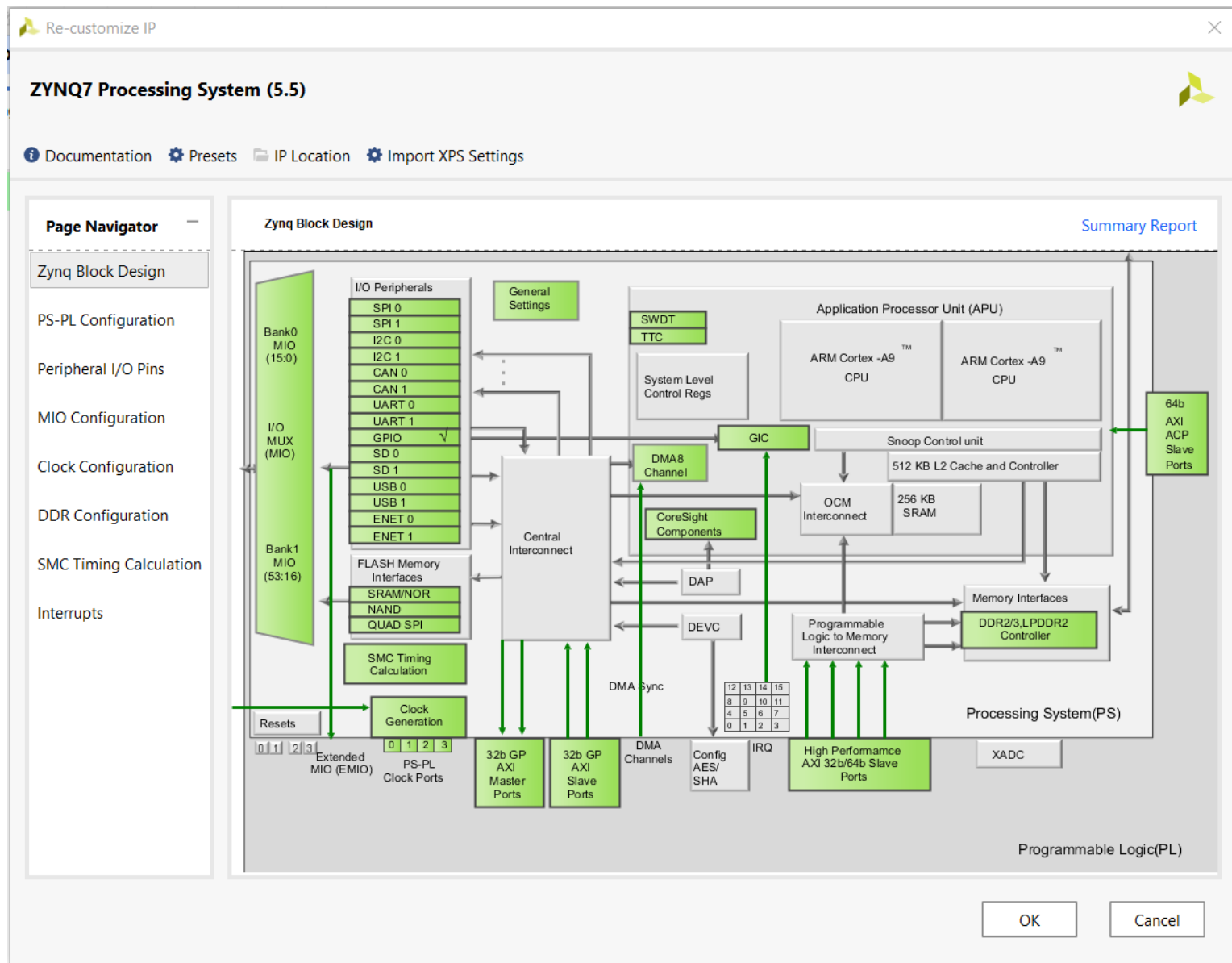


MicroBlaze Core Block Diagram

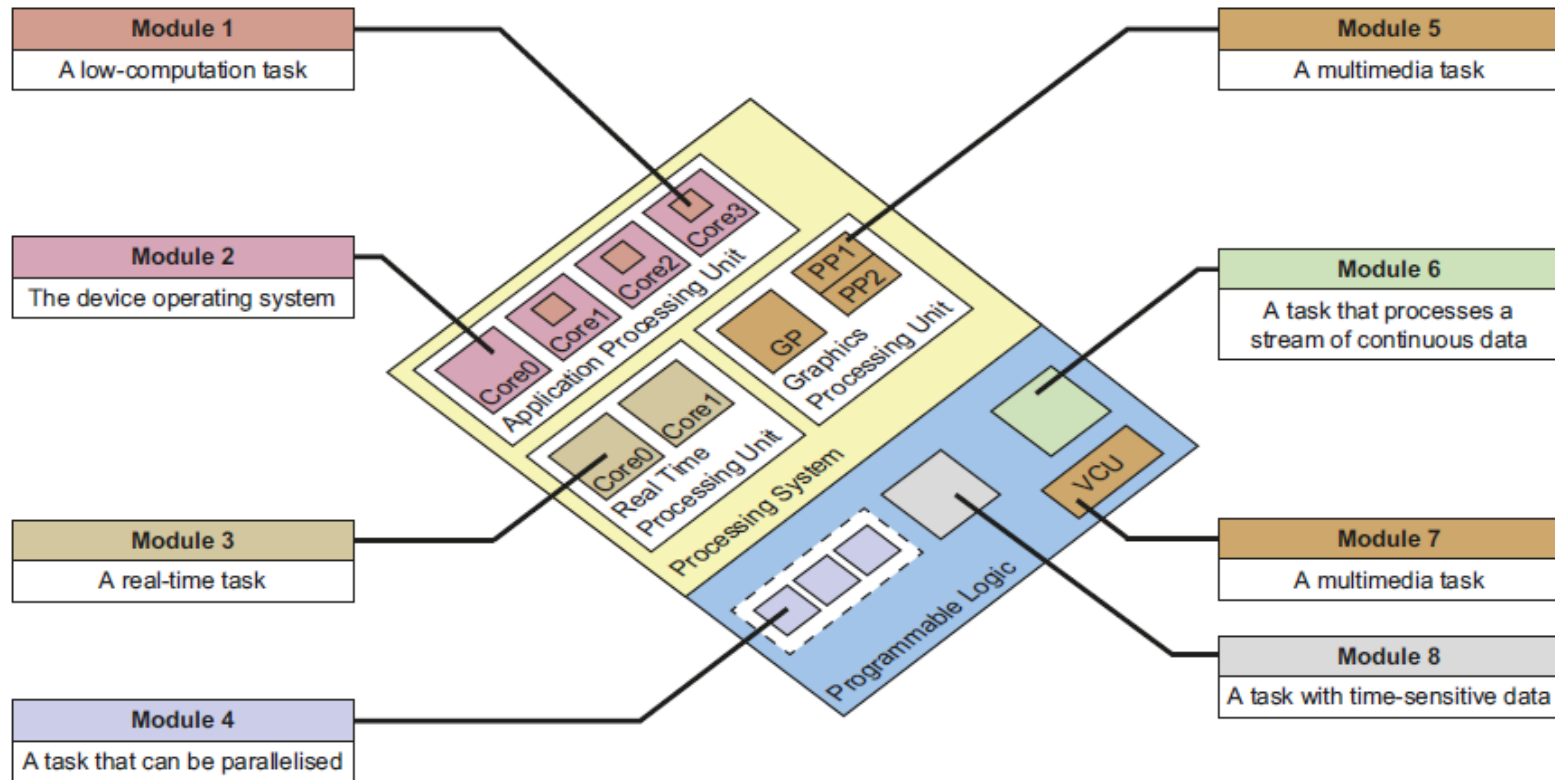
Zynq-7000 AP SoC Block Diagram



Zynq-7000 configuration

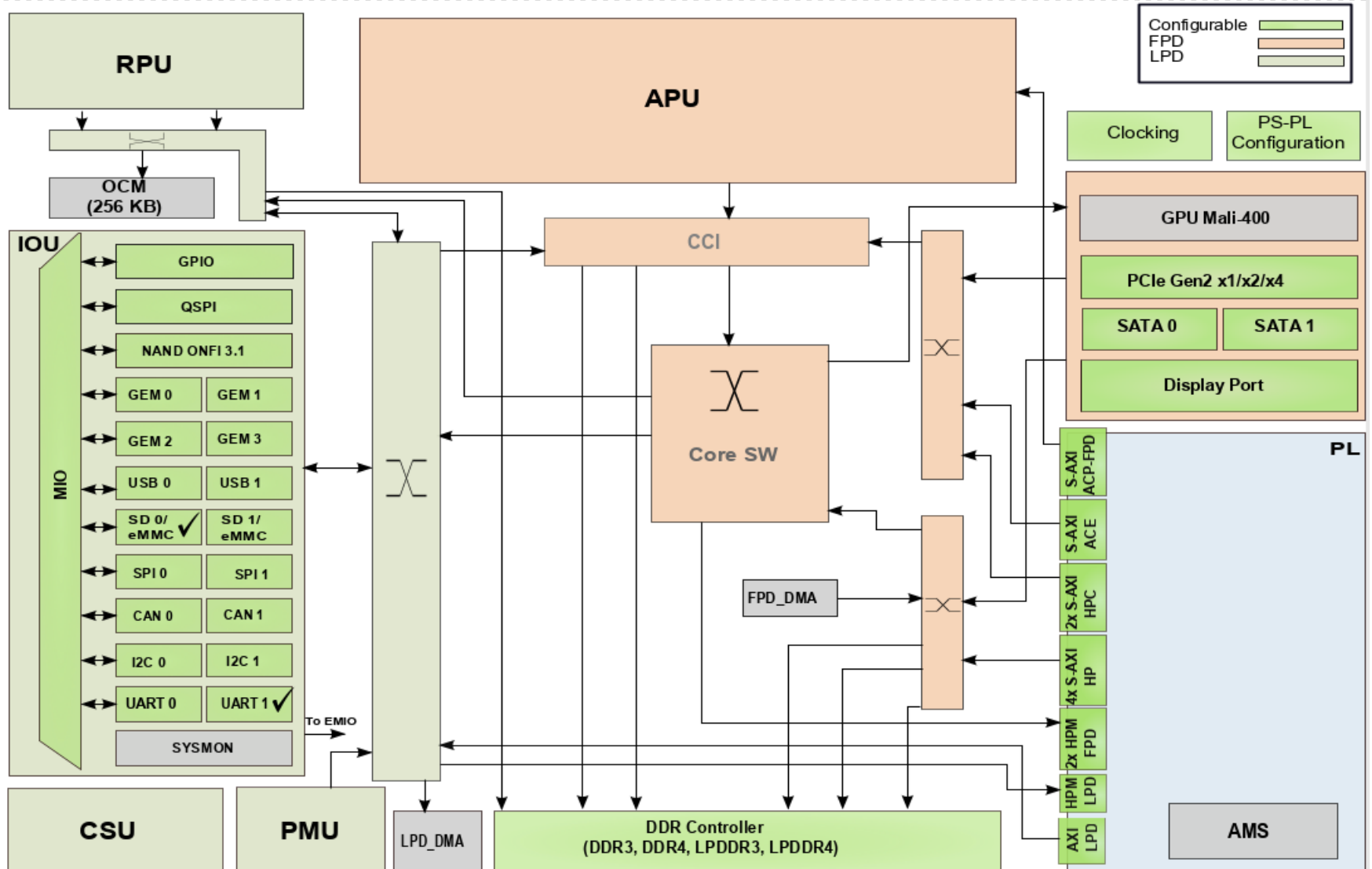


ZYNQ ULTRASCALE



Configuration

PS UltraScale+ Block Design

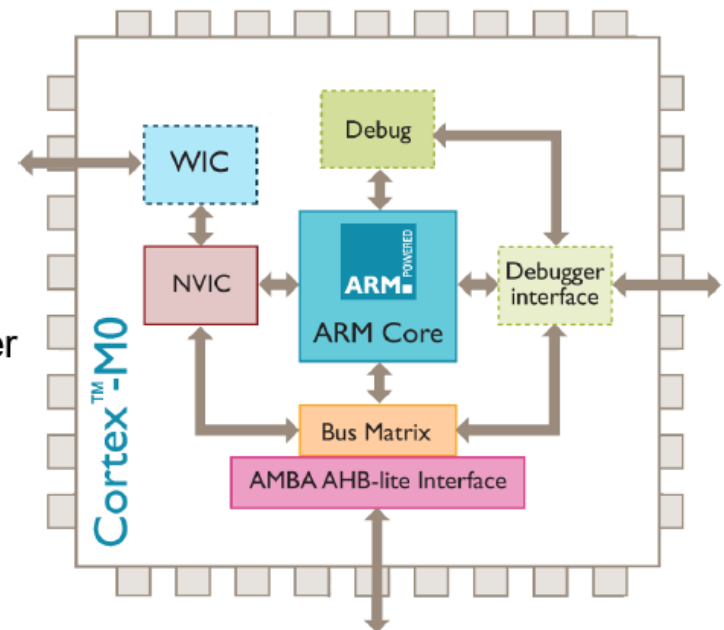


CORTEX FAMILY

ARM Cortex-M0 Processor

- **The smallest, lowest power ARM processor ever**

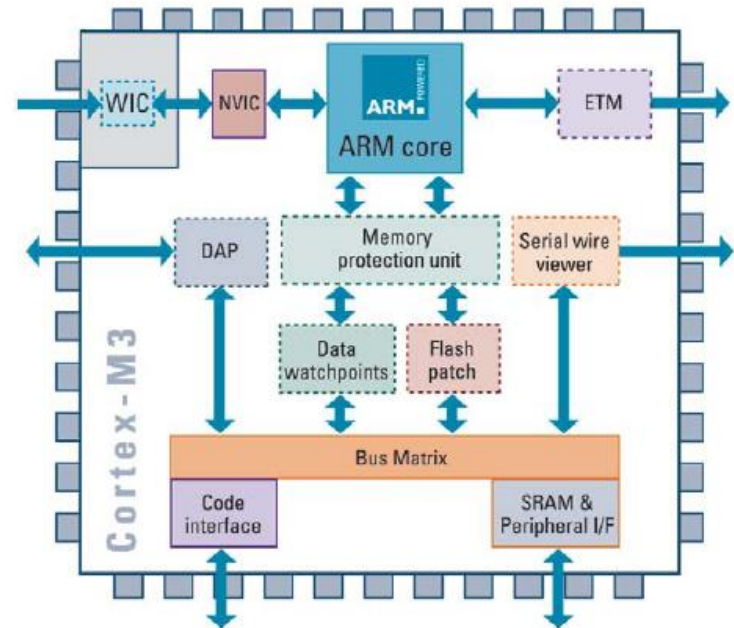
- A third of the area of ARM7TDMI-S
- 85 $\mu\text{W}/\text{MHz}$, 12K gates *
- Von-Neumann bus architecture
- 3-stage pipeline
- Delivers 0.9 DMIPS/MHz
- Configurable nested vectored interrupt controller (NVIC)
- Optional Wake-up Interrupt Controller (WIC)
- Configurable Debug
- Binary and tools upwards compatible with ARM Cortex-M3 processor



Introduction to Cortex-M3 Processor

■ Cortex-M3 Architecture

- Harvard bus architecture
- 3-stage pipeline with branch speculation
- Integrated bus matrix
- Configurable nested vectored interrupt controller (NVIC)
- Advanced configurable debug and trace components
- Optional components for specific market requirements:
 - Wake-up Interrupt Controller (WIC)*
 - Memory Protection Unit (MPU)
 - Embedded Trace Macrocell (ETM)
 - Fault Robust Interface*

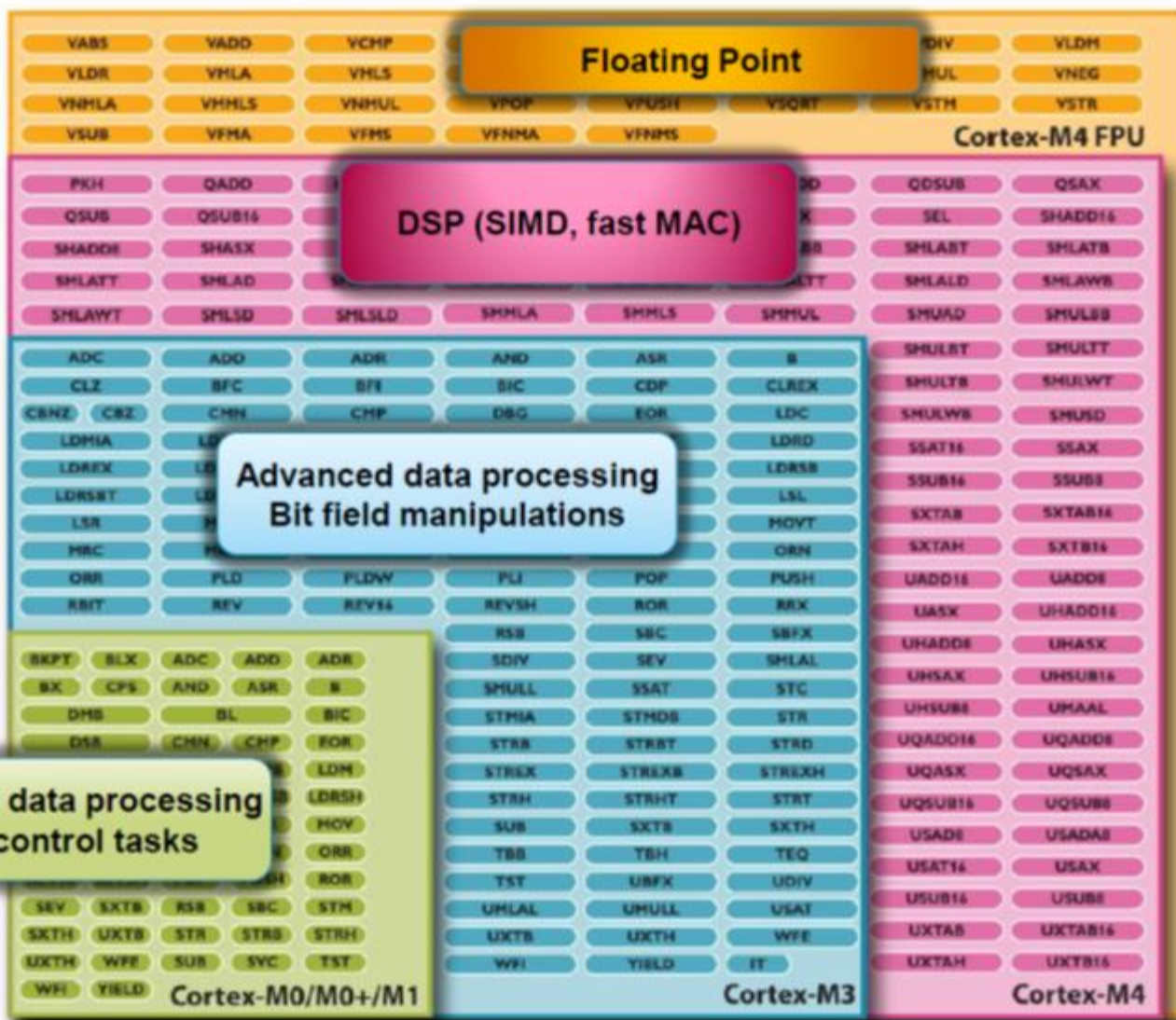


CORTEX-M CORES

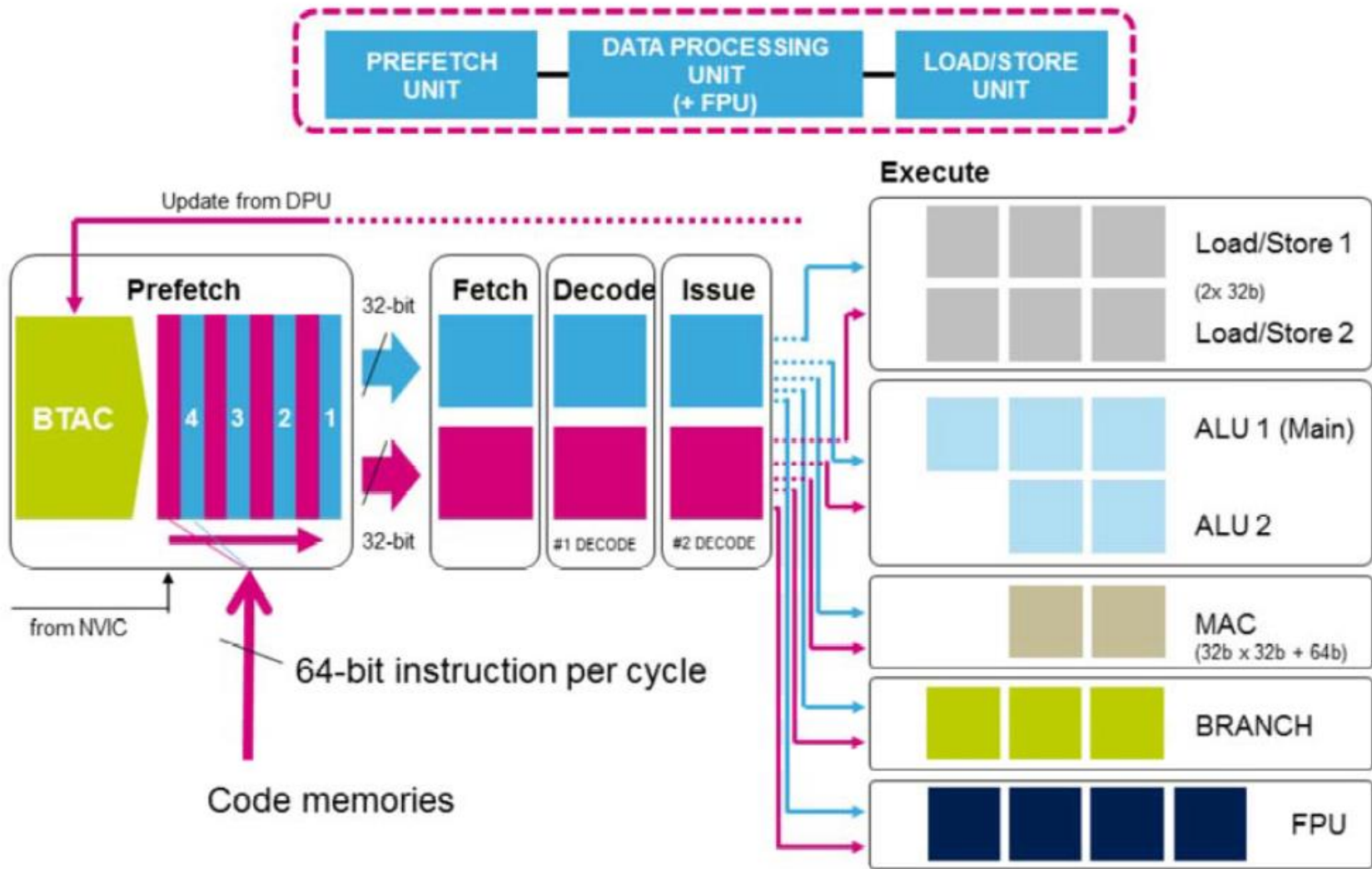
Feature	Cortex-M0	Cortex-M0+	Cortex-M1	Cortex-M23	Cortex-M3	Cortex-M4	Cortex-M33	Cortex-M35P	Cortex-M7
Instruction set architecture	Armv6-M	Armv6-M	Armv6-M	Armv8-M Baseline	Armv7-M	Armv7-M	Armv8-M Mainline	Armv8-M Mainline	Armv7-M
DMIPS/MHz range*	0.87-1.27	0.95-1.36	0.8	0.99	1.25-1.89	1.25-1.95	1.5	1.5	2.14-3.23
CoreMark®/MHz*	2.33	2.46	1.85	2.5	3.34	3.42	4.02	4.02	5.01
Pipeline stages	3	2	3	2	3	3	3	3	6
Memory Protection Unit (MPU)	No	Yes (option)	No	Yes (option) (2 x)	Yes (option)	Yes (option)	Yes (option) (2 x)	Yes (option) (2 x)	Yes (option)
DSP	No	No	No	No	No	Yes	Yes (option)	Yes (option)	Yes
Floating point hardware	No	No	No	No	No	Yes (option SP)	Yes (option SP)	Yes (option SP)	Yes (option SP + DP)
Built-in Caches	No	No	No	No	No	No	No	Yes (option 2-16kB) I-cache	Yes (option 4-64kB) I-cache, D-cache)
Bus protocol	AHB Lite	AHB Lite, Fast I/O	AHB Lite	AHB5, Fast I/O	AHB Lite, APB	AHB Lite, APB	AHB5	AHB5	AXI4, AHB Lite, APB, TCM
Maximum # external interrupts	32	32	32	240	240	240	480	480	240
Hardware divide	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes

The Evolution of the Cortex-M Series

	Cortex-M3	Cortex-M4	Cortex-M7	Traditional DSP
Single cycle MAC		Fixed-point only	Fixed and floating-point	Y
Floating-point		Y	Y	Y
Fractional and saturating math		Y	Y	Y
SIMD operations		Y	Y	Y
Load and store in parallel with math			Y	Y
Zero overhead loops			Y	Y
Accumulator with guard bits				Y
Circular and bit-reversed addressing				Y

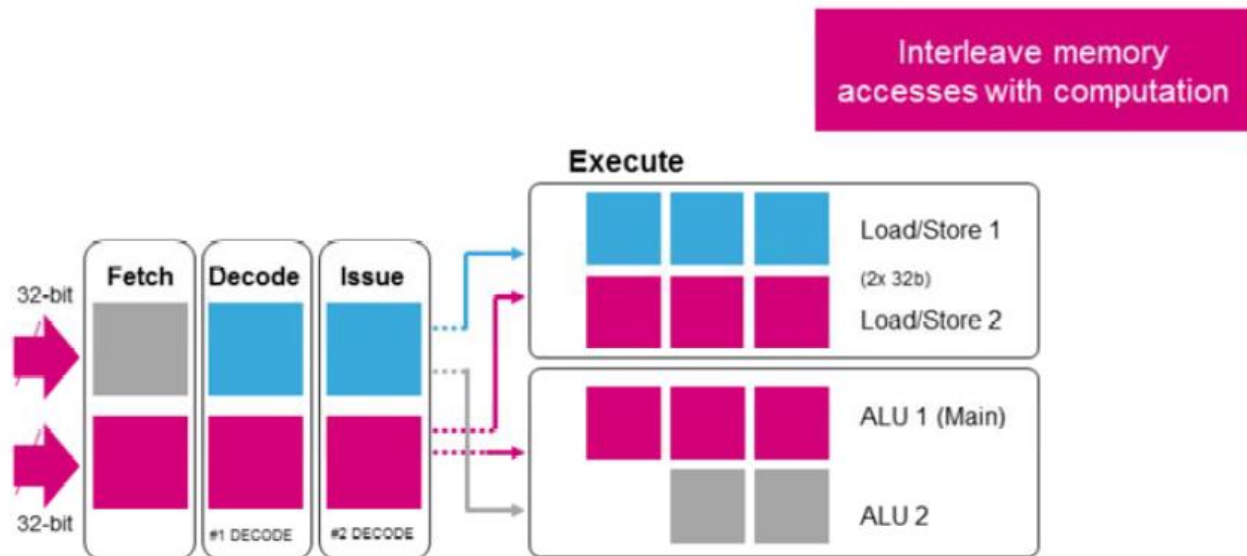


ARM Cortex-M7 → Dual-issue



Load and store in parallel with arithmetic

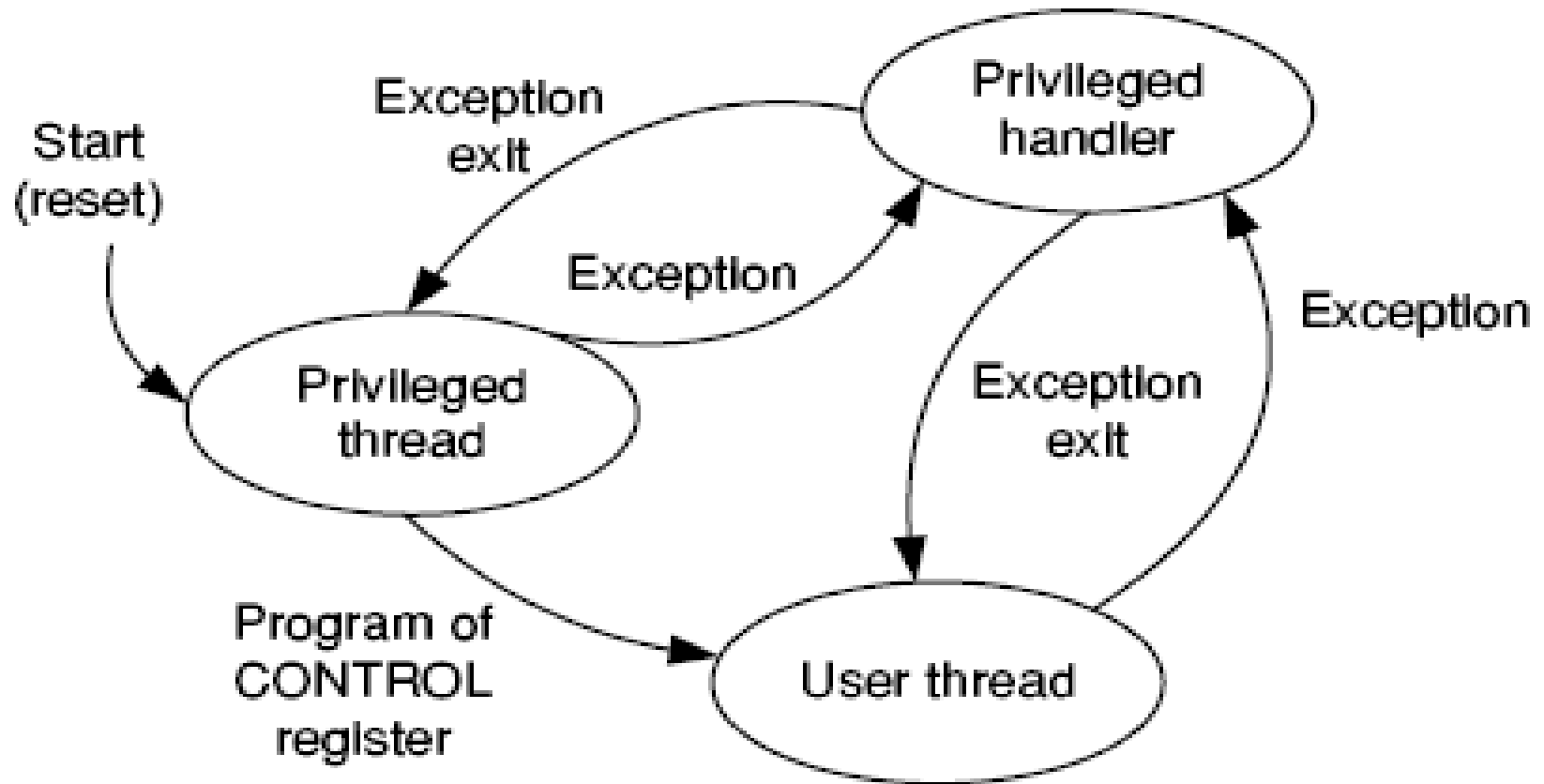
- Cortex®-M7 core
 - Memory access possible without penalty



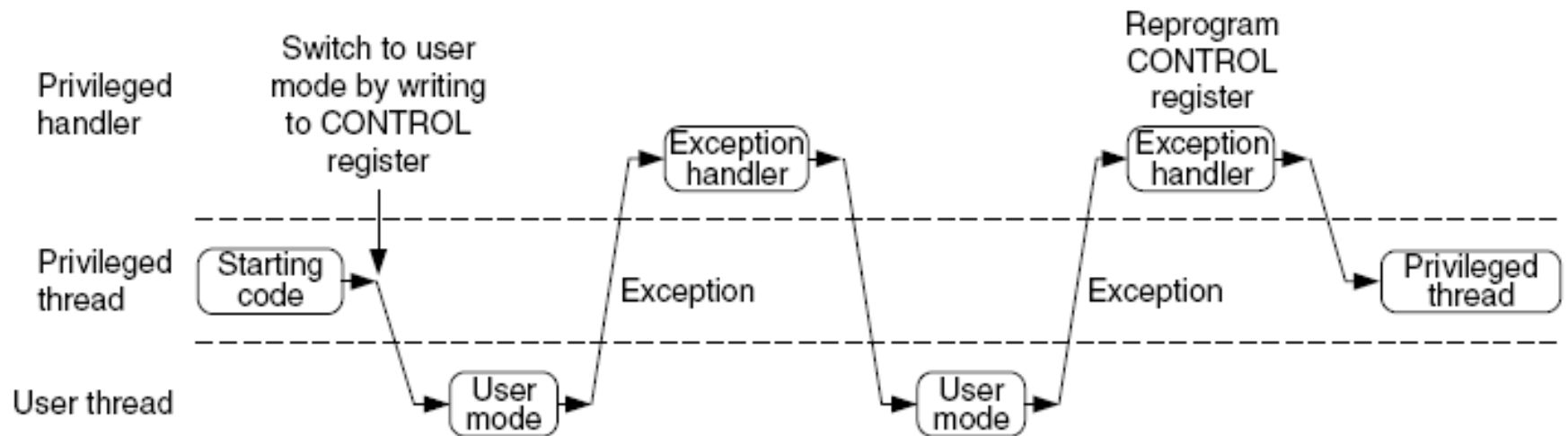
Processor

	Cortex-A5	Cortex-A7	Cortex-A8	Cortex-A9	Cortex-A12	Cortex-A15
Release date	Dec 2009	Oct 2011	July 2006	March 2008	June 2013	April 2011
Typical clock speed	~1GHz	~1GHz on 28nm	~1GHz on 65nm	~2GHz on 40nm	~2GHz on 28nm	~2.5GHz on 28nm
Execution order	In-order	In-order	In-order	Out of order	Out of order	Out of order
Cores	1 to 4	1 to 4	1	1 to 4	1 to 4	1 to 4
Peak integer throughput	1.6DMIPS/MHz	1.9DMIPS/MHz	2DMIPS/MHz	2.5DMIPS/MHz	3.0DMIPS/MHz	3.5DMIPS/MHz
Pipeline stages	8	8	13	9 to 12	11	15+
Instructions decoded per cycle	1	Partial dual issue	2 (Superscalar)	2 (Superscalar)	2 (Superscalar)	3 (Superscalar)
Floating Point Unit	Optional	Yes	Yes	Optional	Yes	Optional
AMBA interface	64-bit AMBA 3	128-bit AMBA 4	64 or 128-bit AMBA 3	2× 64-bit AMBA 3	128-bit AMBA 4	128-bit AMBA 4

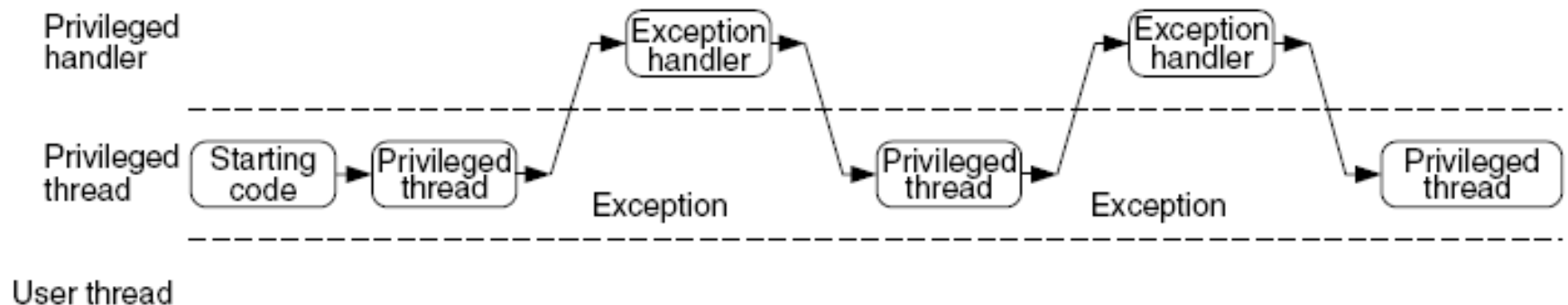
CORTEX MCU Modes



CORTEX Operation modes

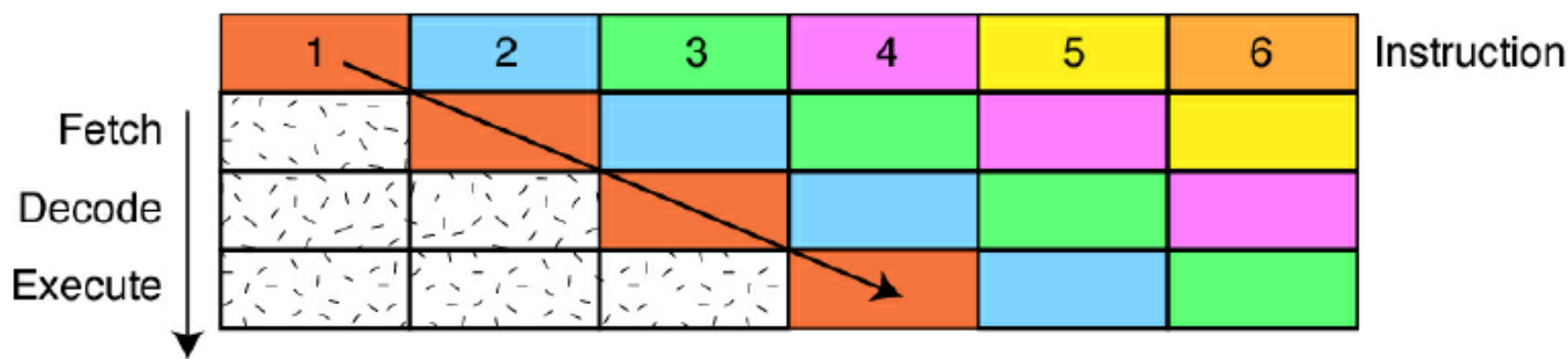


Switching of Operation Mode by Programming the Control Register or by Exceptions.



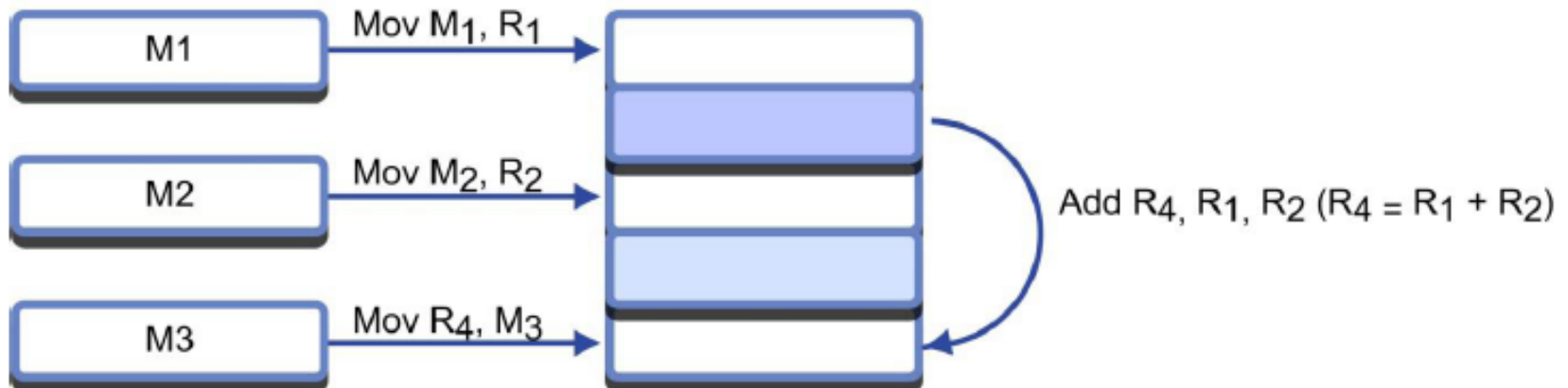
Instruction pipeline

- Each instruction is processed in a number of discrete steps
- Multiple instructions can be processed simultaneously by starting processing of the next instruction before the last has finished.

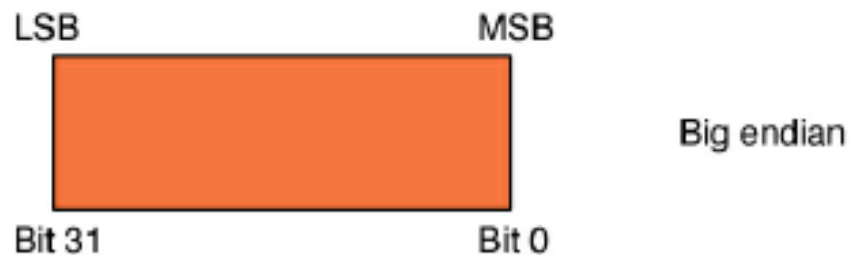
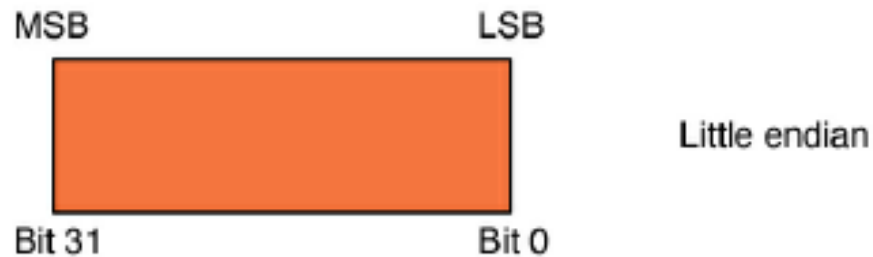


Load-And-Store Architecture

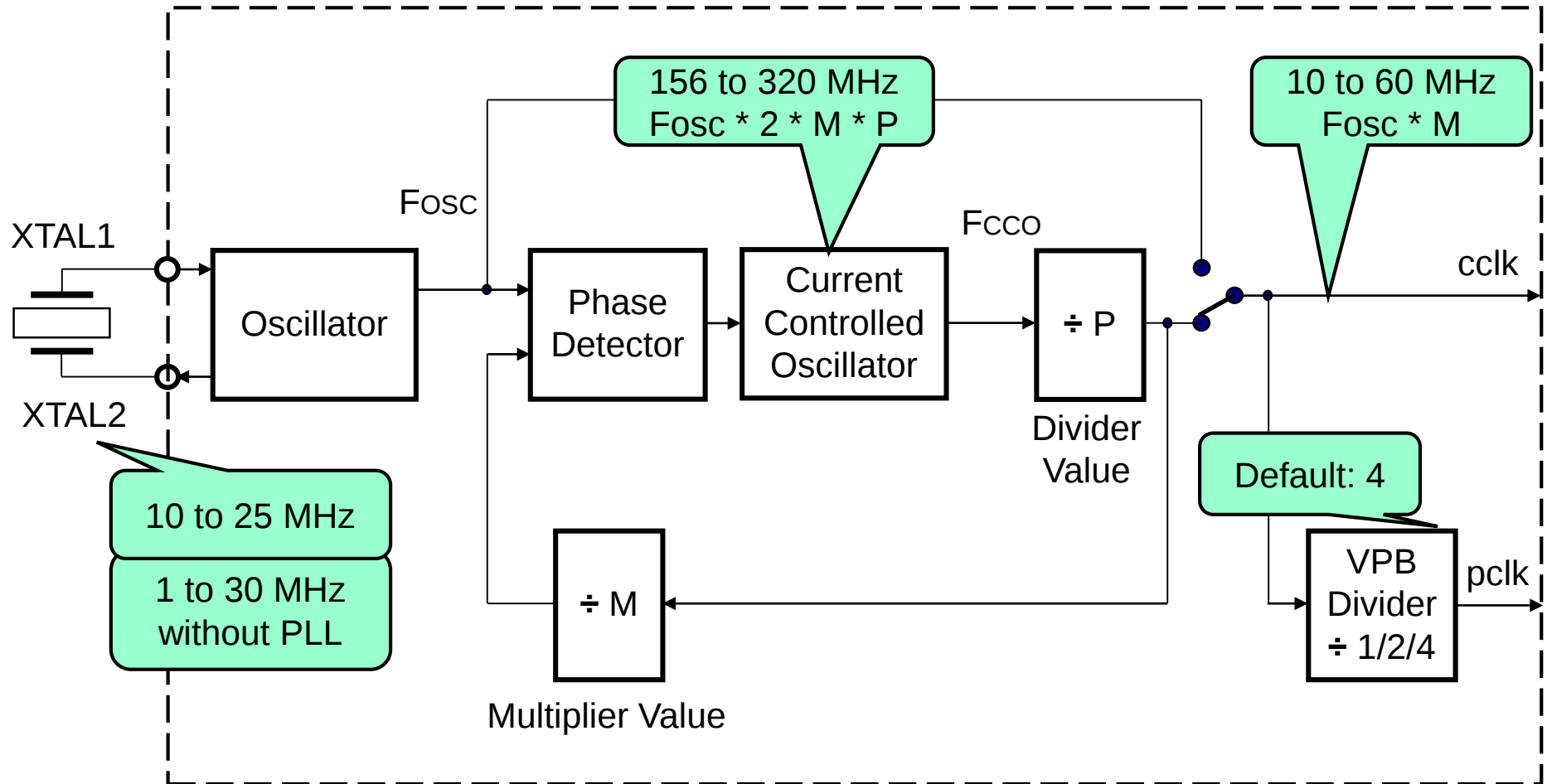
The Cortex CPU is a RISC processor which has a load and store architecture. In order to perform data processing instructions, the operands must be loaded into a central register file, the data operation must be performed on these registers and the results then saved back to the memory store.



ARM Memory organisation



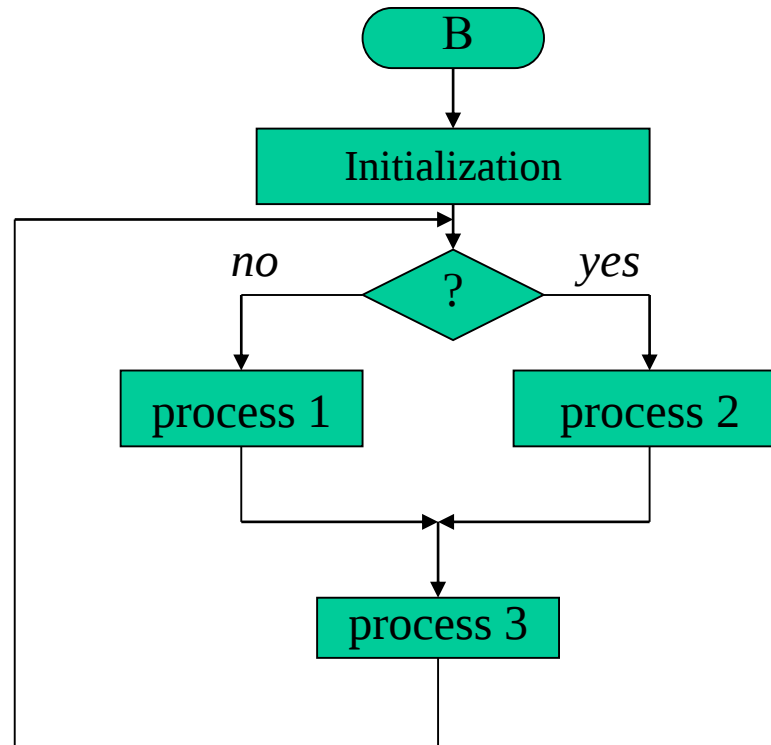
Phase Locked Loop



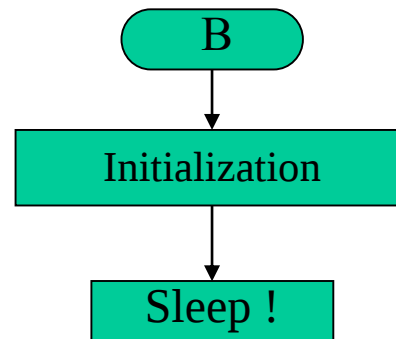
Programming tips



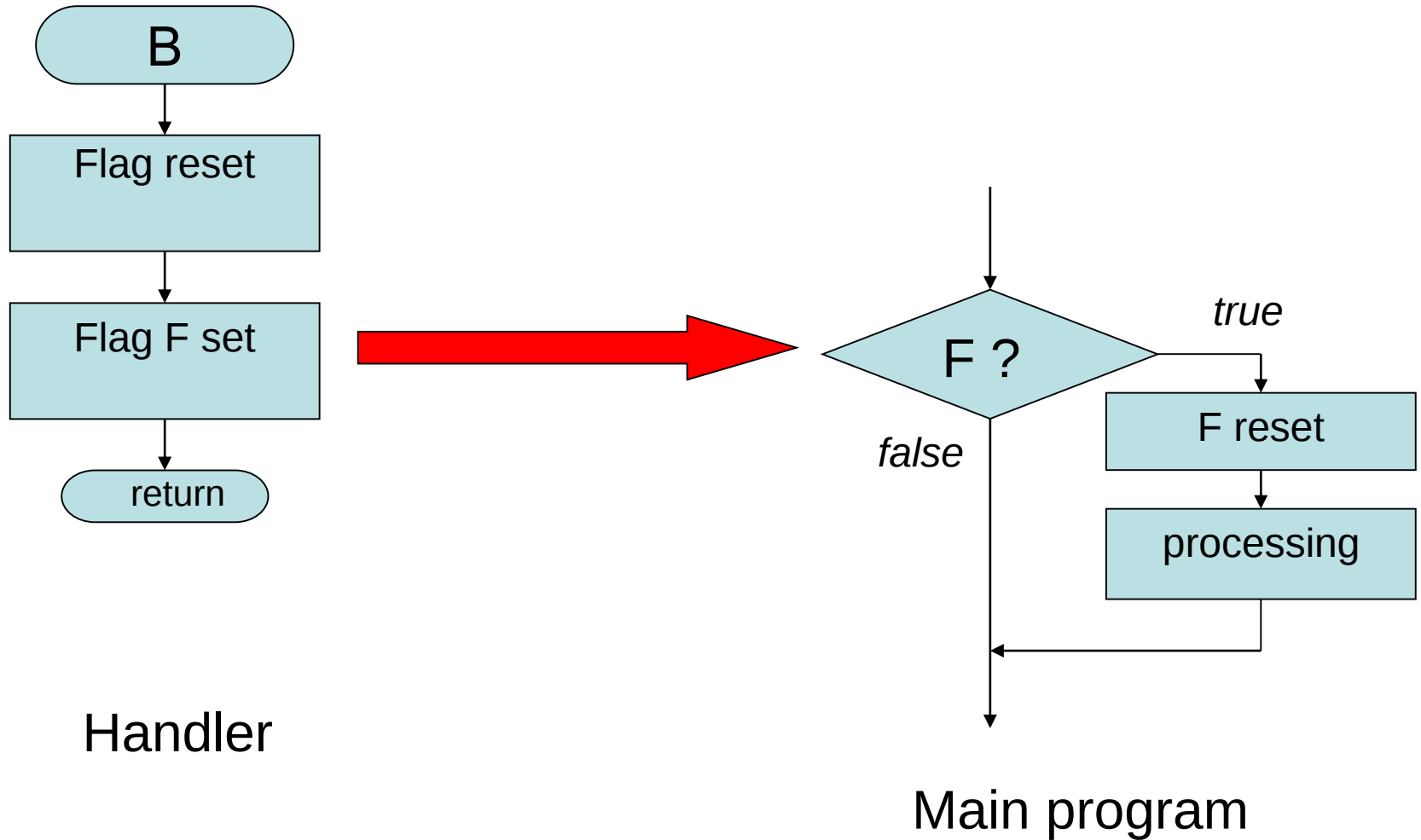
Programming tips



Programming tips



Sharing functionality



- Do we need an operating system?

Operating systems

Advantages:

- Developer can use built-in features;
- Less software dependency on hardware;
- Interfaces;
- Multitasking and protection.

Drawbacks:

- Code size increases;
- Efficiency can decrease;
- Dependency on OS principles and features.

Operating systems

- General purpose operating systems (GPOS) – Windows, Unix, etc.
- Real-time operating systems (RTOS) – QNX, FreeRTOS, Salvo, uC/OS etc.

Operating systems

General purpose operating systems (GPOS)

Real-time operating systems (RTOS)

Windows, Unix, Linux, etc.

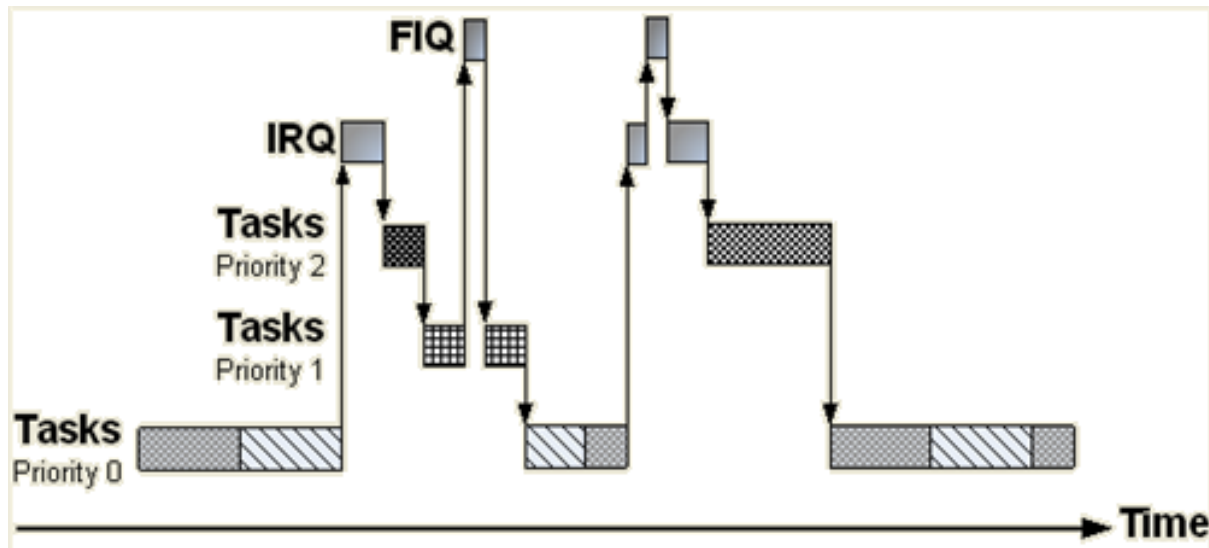
QNX, FreeRTOS, Salvo, uC/OS etc.

Designed to do many things but are not designed to offer strict guarantees of:

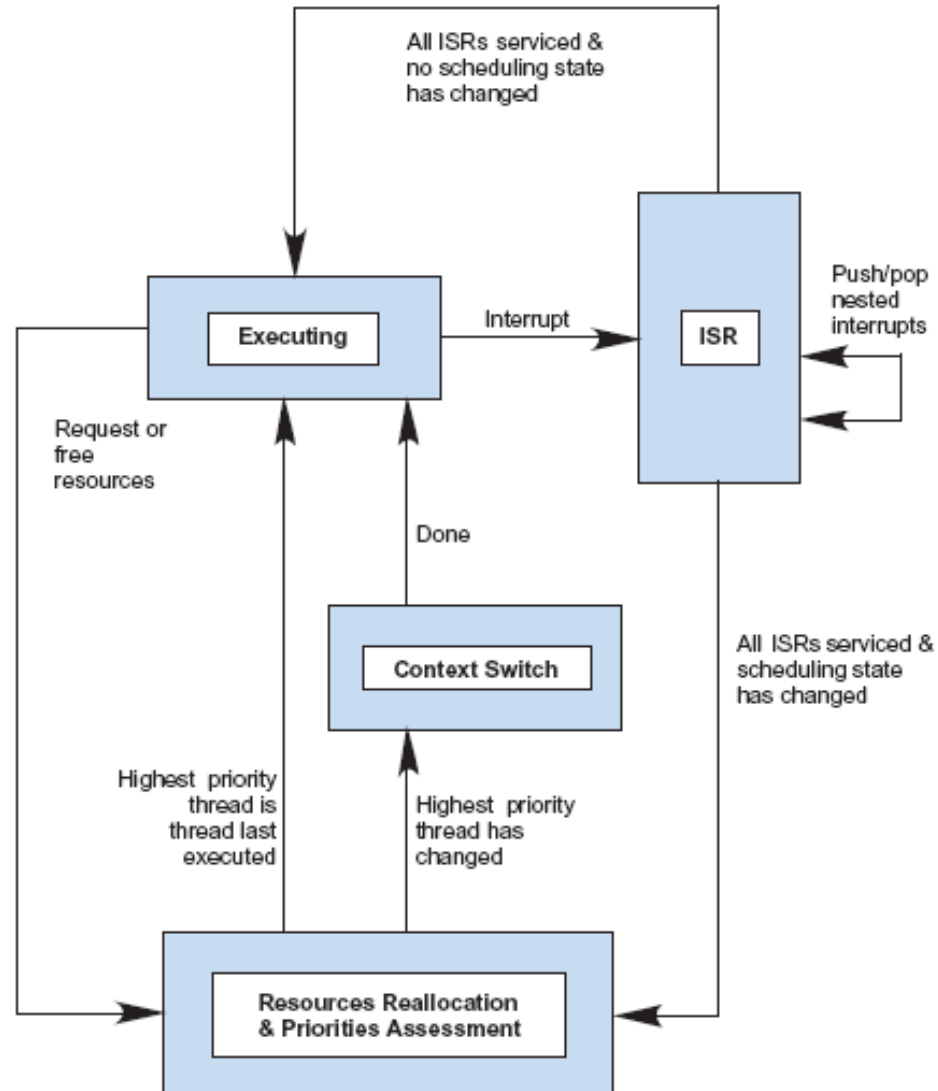
- availability (how often the system responds to requests in a timely manner)
- reliability (how often these responses are correct)

Engineered to guarantee:

- availability
- reliability



VDK



Drivers

